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REMARKS

Claims 1-25 are pending in this Application, of which Claims 1, 7, 12, 14, 18 and 22 are the independent claims. All claims stand rejected.

Claims 1, 7, 12 and 18 are being amended to further clarify the scope of the claims, by reciting (in the same or similar language) that the "plurality of serial registers" are "each associated with a different one of the plurality of input ports," and that "each of the serial registers" is "configured for simultaneously receiving packet data from the associated input port." Support for this amendment is found at least at Fig. 7 and page 10, lines 10-20 of the Specification as originally filed. Here, with reference to Fig. 7, it is stated that "thirty-two I/O ports 70 each connect to an associated one of thirty-two serial registers 72" (emphasis added). It can be seen in Fig. 7 that serial register 72 (e.g., "serial register 0") is associated with only one of the ports (e.g., "IO PORT 0") as shown by a signal path between the port and serial register, and does not have connectivity with any other of the ports (e.g., "IO PORT 31"). Thus, each of the serial registers is associated with "a different one of the plurality of input ports."

Claim 1 is also being amended to recite "each of the serial registers further being segmented into a plurality of segments." Support for this amendment is found at least on page 13, lines 10-22 and Figs. 7 and 8 of the Specification as originally filed.

Claims 14-17 are directed to a "method for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device," which includes, among other features, "storing the packet in a physical location of a memory array of the PBRAM device," "storing a pointer to the physical location in an entry of a packet table in the memory array," and "storing a pointer to the entry in the packet table in an input queue structure." It is believed that Claims 14-17 are directed to an invention that is distinct from the other claims pending in this Application. Thus, Applicant suggests a Restriction of the pending claims, where Group I comprises Claims 1-13 and 18-21, and Group II comprises Claims 14-17. If such a restriction is granted, Applicant elect Group I (Claims 1-13 and 18-21) for consideration.

Claims 22-25 are being cancelled to expedite consideration of the remaining claims. Applicants reserve the right to file the cancelled claims in a continuation or divisional application claiming priority to the present application.

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Rejection of Claims 1-25 under 35 U.S.C. 102(b) and 35 U.S.C. 103(a)

The Office Action substantially maintains the rejections raised in the previous Office Action mailed on April 3, 2007, holding that Claims 1, 2, 7, 12, 14, 18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Toda et al. (U.S. Patent No. 5,612,925). In response to Applicant's arguments, the Office Action asserts, on page 8, that "in Toda's invention the number of input/output ports is irrelevant since the plurality of input ports can be connected through a data bus or an interface that combines the data coming from the plurality of input ports and output them serially as taught by the invention of Balmforth" (emphasis added).

In Toda (Fig. 16), the single I/O DATA port 164 could be connected to interface with a plurality of additional ports. However, no such additional ports are disclosed in Toda, and so it is believed that the § 102 rejection of Claims 1, 2, 7, 12 and 18 is improper. Furthermore, even if Toda were modified to receive data from multiple ports at the I/O DATA port 164, all of those multiple ports would be associated with the single serial register section 167. In contrast, in the present invention, each of the plurality of serial registers is associated with a different one of the plurality of input ports. An example embodiment, shown in Fig. 7 of the Specification, shows several serial registers 72, each of which are associated with a different I/O port 70. For example, "Serial Register 0" has connectivity only with "IO PORT 0," and "Serial Register (31)" has connectivity only with "IO Port 31." No such configuration is disclosed by Toda; nor is it suggested by Balmforth or any combination of Toda and Balmforth.

Further, amended claim 1 now recites that "each of the serial registers [is] configured for simultaneously receiving packet data from the associated input port and writing packet data," and that "each of the serial registers" is "segmented into a plurality of segments." Toda does disclose a serial register 167 having a plurality of segments. Yet claim 1 of the present Application recites a plurality of serial registers each having a plurality of segments, and where each serial register can receive packet data from a different associated port. As illustrated in Applicant's Figs. 7 and 8, each serial register 72 (Fig. 7) is shown in further detail in Fig. 8, where the serial register 72 has eight 256-bit segments. Each of the thirty-two serial registers 72 in Fig. 7 is segmented in this way, thereby forming a "plurality of serial registers" as now recited in Claim 1.

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In view of the above, it is believed that Claims 1, 2, 7, 12 and 18 as now amended distinguish over Toda. As a result, the § 102 rejection of Claims 1, 2, 7, 12 and 18 is traversed, and reconsideration is respectfully requested.

Due to the aforementioned shortcomings of Toda, one skilled in the art would find no suggestion of the invention as recited in dependent claims 6, 11, 13, and 21. Thus, the § 103 rejection of claims 6, 11, 13, and 21 is traversed.
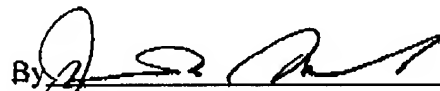
Claims 3-5, 8-10, 19 and 20 depend from one of base Claims 1, 7, 12, and 18, and thus are distinct from Toda for the aforementioned reasons. Zuravleff provides no suggestion of a plurality of input ports for receiving packet data that is stored to a shared memory. Therefore, no combination of Toda and Zuraleff teaches or suggests the present invention, and the § 103 rejection of Claims 3-5, 8-10, 19 and 20 is believed to be overcome; Applicant respectfully requests reconsideration.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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